Amendments to the Claims

Amend claims 1 - 10 as follows:

1. (Currently Amended) ~~A circuit used in modeling integrated circuits which comprises:~~ An integrated circuit device comprising elements, wherein the elements comprise characteristics and parameters in accordance with a circuit model, wherein the circuit model comprises:

at least one output node;

a first and second current function;

a first voltage function;

a first, second, and third capacitance function; and

an internal impedance function,

wherein the output node has a value that is a function of the first and second current function, the first voltage function, the first, second and third capacitance functions and the internal impedance function collectively.

~~a first current source connecting an output node to a voltage supply; and a second current source connecting an the output node to a ground;~~

~~a Miller capacitor connected to an input node and the output node;~~

~~an input capacitor connected to the input node and to ground; and~~

~~an output capacitor and internal impedance, Zint, connected to the output node and ground.~~

2. (Currently Amended) The circuit device of claim 1 [[where]] wherein the first and second current [[sources]] functions are [[full]] subsequently functions of the [[an]] input node voltage value and the output node voltage value ~~input and output voltages~~.

3. (Currently Amended) The circuit device of claim 2 [[where]] wherein the first, second, and third capacitance functions ~~the capacitance of each capacitor~~ and the impedance function are ~~of Zint are assumed to be full~~ each functions of the input and output voltage values.

4. (Currently Amended) The circuit device of claim 1, further comprising:

an output load function, wherein the output load function is a function of a near capacitor function, a resistor function, and a far capacitor function, collectively.

~~which has an output load, Zload, which comprises three elements a near capacitor, a resistor and a far capacitor..~~

5. (Currently Amended) The circuit device of claim [[3]] 1, wherein the first current function is a function of a p-block behavioral model, and the second current function is a function of an n-block behavioral model. ~~where the first current source represents the p transistor and the second current represents the n transistor.~~

6. (Currently Amended) The circuit device of claim 5 wherein the first current function is a function of each of the input and output node values, collectively. ~~where a current source when there are multiple inputs.~~

7. (Currently Amended) The circuit device of claim 5 wherein a first current function is configured to be functionally dependent on a first plurality of input node voltage values and a second plurality of output node voltage values, and a second current function is configured to be functionally dependent on a third plurality of input node voltage values and a fourth plurality of output node voltage values. ~~where each current source could be spit up into an arbitrary number of parallel current sources, each of which could depend on a different set of inputs, in addition to the output of interest.~~

8. (Currently Amended) A circuit device comprising elements, wherein the elements comprise characteristics and parameters in accordance with a circuit model, wherein the circuit model comprises:
~~A circuit used in modeling integrated circuits, which comprises:~~

an ideal current source connecting an output node to a voltage supply;

a [[Miller]] first capacitor connected to [[an]] the input node and the output node;

an input capacitor connected to the input node and to ground; [[and]]

an output capacitor connected to the output node and ground; and

an internal impedance, [[Zint,]] connected to the output node and ground.

9. (Currently Amended) The circuit device of claim 8 [[where]] wherein the ideal current source, ~~is a full function of the input and output voltages and where~~ the capacitance of each capacitor and the internal impedance [[of Zint]] are ~~assumed to be full~~ each functions of the input node and output node voltage.

10. (Currently Amended) The circuit device of claim 9, further comprising [[which has]] an output load, ~~Zload, which comprises~~ having a near capacitor, a resistor, and a far capacitor.

11. (Withdrawn) A method of modeling an IC that provides output waveforms, comprising the steps of:

translating a model of the IC comprising ideal current sources and capacitors into a differential equation which is implicit with respect to output voltages;

supplying values of the model's elements at a sufficient I/O voltages to cover the desired range of I/O node voltages;

resimulating the model by solving the differential equation through an ODE solver, given an input waveform, the element values and an output load.

12. (Withdrawn) The method of modeling an IC of claim 11 also comprising the step of:

storing generalization equations and solving the generalization equations to obtain model element values.

13. (Withdrawn) The method of modeling an IC of claim 11 also comprising the step of:

performing measurements in order to obtain the model element values.

14. (Withdrawn) The method of claim 11 also comprising the steps of:

interpolating of element values in the space of I/O node voltages;

manipulating element values such as time or voltage-threshold-based delay, averaging or clipping.

15. (Withdrawn) The method of claim 12 also comprising the step of:

solving the generalization equations using interpolated parameters and externally specified environmental parameters to obtain model element values.

16. (Withdrawn) The method of claim 11 also comprising the step of:

at each time step during solution of the ODE, determining the output load by having the ODE solver call a callback function requesting the load current by providing to the callback function the time and output node voltage.

17. (Withdrawn) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform method steps for modeling an IC, the method steps comprising:

translating a model of the IC comprising ideal current sources and capacitors into a differential equation which is implicit with respect to output voltages;

supplying values of the model's elements at a sufficient I/O voltages to cover the desired range of I/O node voltages;

re-simulating the model by solving the differential equation through an ODE solver, given an input waveform, the element values and an output load.

18. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

storing generalization equations and solving the generalization equations to obtain model element values.

19. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

performing measurements in order to obtain the model element values.

20. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

interpolating of element values in the space of I/O node voltages;

manipulating element values for environmental parameters such as time or voltage-threshold-based delay, averaging, or clipping.

21. (Wtihdrawn) The program storage device of claim 18 wherein the method steps also comprise:

solving the generalization equations using interpolated parameters and externally specified environmental parameters to obtain model element values.

22. (Withdrawn) The program storage device of claim 17 wherein the method steps also comprise:

at each time step of the input waveform, determining the output load by having the ODE solver call a callback function requesting the load current by providing to the callback function the time and output node voltage.